



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,406	01/23/2004	Paul F. Newman	110348-134857	9510

31817 7590 01/29/2007  
SCHWABE, WILLIAMSON & WYATT, P.C.  
PACWEST CENTER, SUITE 1900  
1211 S.W. FIFTH AVE.  
PORTLAND, OR 97204

EXAMINER
----------

SUGENT, JAMES F

ART UNIT	PAPER NUMBER
----------	--------------

2116

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/764,406	NEWMAN, PAUL F.	
	<b>Examiner</b>	<b>Art Unit</b>	
	James F. Sugent	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☒ Responsive to communication(s) filed on 24 November 2006.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-4, 7-11, 14-18, 21, 22, 28 and 30-32 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)          | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

### **DETAILED ACTION**

This Office Action is sent in response to Applicant's Communication received November 24, 2006 for application number 10/746,406 originally filed January 23, 2004. The Office hereby acknowledges receipt of the following and placed of record in file: amended claims 1-32 wherein claims 5, 6, 12, 13, 19, 20, 23-27 and 29 are canceled.

#### ***Claim Objections***

Examiner herein acknowledges amendment to claim 8 and finds the claim objection (from Office Action submitted October 25, 2006) to be overcome.

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

Art Unit: 2116

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-4, 7-11, 14-18, 21, 22, 28 and 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barkatullah et al. (U.S. Patent No. 6,104,219) (hereinafter referred to as Barkatullah) in view of Neal et al. (U.S. Patent No. 5,946,470) (hereinafter referred to as Neal).

As to claim 1, Barkatullah discloses an apparatus, comprising: a clock source to generate a clock signal (102); a first circuit (core 101), coupled to a first clock domain (core clock), to generate a first data signal and a second circuit (interface 105 and external devices) coupled to a second clock domain (bus clock) (clock generator 102 creating core and bus clock signals; column 4, line 66 thru column 5, line 25); a flip-flop (comprised of D flip-flop outside of pad cell 831 hereinafter referred to as DFF1 and D flip-flop on the left inside of pad cell 831 hereinafter referred to as DFF2 in Fig. 8C), having a pair of inputs coupled to the clock source (core clock) and the first circuit (core clock domain), to generate a second data signal (Q output of DFF2 hereinafter referred to as Q2) in response to the clock signal (core clock) and the first data signal (data from core clock domain); a clock production circuit (Fig. 7) coupled to the clock source (102) and responsive to the clock signal (core clock) to generate a synchronized clock signal (bus clock) having a triggering clock edge (column 8, line 39 thru column 9, line 24); a downstream latch (D flip-flop on the right inside of pad cell 831 in Fig. 8C hereinafter referred to as DFF3), having an open state and a close state (inherent to flip-flops), a pair of inputs coupled to DFF2 and the clock production circuit (Fig. 7) and an output (Q output hereinafter referred to as Q3) coupled to the second circuit (interface 105 to devices external), to generate an output data signal (Q3) in response to the core data signal (Q2) and the synchronized clock signal (bus clock), with the triggering clock edge of the bus clock signal switching the downstream latch from the close

Art Unit: 2116

state to the open state (column 9, lines 36 thru column 10, line 13); and, wherein the Q2 data signal has a plurality of rising and falling data edges (inherent to data signals) and the clock production circuit (Fig. 7) is operable to synchronize an arrival of the triggering clock edge at the downstream latch until after an arrival of the rising and falling data edges at the downstream latch (column 4, line 66 thru column 5, lines 25 and column 8, line 39 thru column 9, line 24 and column 9, lines 36 thru column 10, line 13).

Barkatullah fails to disclose: the first circuit, coupled to a first supply voltage source and the second circuit coupled to a second supply voltage; a first level shifter to generate a level shifted data signal in response to the second data signal; and, a second level shifter and a delay element both coupled to the clock source to create delayed, level-shifted clock signal.

Neal teaches a method and system (Fig. 6) for use in a computer system between a processor domain (140 within processor package) and a chipset for I/O of the processor (400) to be used for level-shifting between the two domains (processor voltage domain V2 and I/O domain V2) with a clock delaying mechanism (150) to synchronize clock triggering. Neal features a first domain/circuit (400) which produces data signals (401a-403a) that are transmitted through a level-shifter (101) to produces level-shifted data signals (401b-403b) (from domain V1 to domain V2; column 5, line 59 thru column 6, line 29). Neal further teaches a clock source (160) that is used by first domain (400) to synchronize data signals (401a-403a) wherein the clock signal is further level-shifted (via 101) and delayed via delay element (150) (column 5, lines 15-58). Neal further teaches the additional benefit of providing a level-shifting technique to be used for a upgrading a board without need for redesigning the board (column 3, lines 1-4).

Art Unit: 2116

It would have been obvious to one of ordinary skill of the art having the teachings of Barkatullah and Neal at the time the invention was made, to modify the apparatus of Barkatullah to include the ability to level-shift both data and clock signals as well as delay the clock signal between domains for synchronization as taught by Neal. One of ordinary skill in the art would be motivated to make this combination of including the level-shifting of data and clock signals and deskewing of the clock signal in view of the teachings of Neal, as doing so would give the added benefit of providing a level-shifting technique to be used for a upgrading a board without need for redesigning the board (as taught by Neal above).

As to claim 2, Barkatullah in combination with Neal taught the apparatus in claim 1, as shown above. Neal further teaches the apparatus further comprising: a second level shifter (all inclusive within 101), coupled between the clock source and the downstream latch (as discussed hereinabove) and in series with the delay element (column 5, line 59 thru column 6, line 29).

As to claim 3, it is directed to the apparatus of steps set forth in claim 2. Therefore, it is rejected for the same basis as set forth hereinabove.

As to claim 4, Barkatullah in combination with Neal taught the apparatus in claim 1, as shown above. Neal further teaches the apparatus wherein the delayed clock signal has a plurality of clock cycles with each of the clock cycles having a rising clock edge and a falling clock edge (inherent to clock signals).

Barkatullah further teaches the downstream latch (as discussed hereinabove) is switched from the close state to the open state by the triggering clock edge selected from the rising clock edge and the falling clock edge and switched from the open state to a close state by the non-

Art Unit: 2116

selected clock edge of the rising clock edge and the falling clock edge (column 9, line 36 thru column 10, line 43).

As to claims 7-9, they are directed to the apparatus of steps set forth in claim 4.

Therefore, they are rejected for the same basis as set forth hereinabove.

As to claim 10, Neal discloses an apparatus, comprising: a microprocessor (100) including a central processing unit section (101) having a first clock domain (core clock); an input-output section (105) having a second clock domain (bus clock); a clock source (102) to generate a clock signal (core clock and bus clock) (column 4, line 66 thru column 5, lines 25); and a selected section (D flip-flop outside of pad cell 831 in Fig. 8C hereinafter referred to as DFF1) of the CPU section and the I/O sections being operable to generate a first data signal, with the selected section providing a first data signal (output Q hereinafter referred to as Q1); a converter circuit including a flip-flop (D flip-flop on the left inside of pad cell 831 in Fig. 8C hereinafter referred to as DFF2), coupled to the clock source (core clock) and the selected section (DFF1), to generate a second data signal (Q output hereinafter referred to as Q2) in response to the clock signal and the first data signal (Q1); a clock production circuit (Fig. 7) coupled in series to the clock source (102), to generate a clock signal with a triggering clock edge (bus clock) in response to the clock signal (column 8, line 39 thru column 9, line 24); a downstream latch (D flip-flop on the right inside of pad cell 831 in Fig. 8C hereinafter referred to as DFF3) having an open and close state (inherent to flip-flops), a pair of inputs coupled to DFF2 and the clock production circuit (Fig. 7) and an output (Q output hereinafter referred to as Q3) coupled to the non-selected section of the CPU and I/O sections (external devices); the downstream latch adapted to generate an output data signal (Q3) in response to the data signal (Q2) and the

Art Unit: 2116

triggering clock edge of the synchronized clock signal (bus clock) (column 9, lines 36 thru column 10, line 13); and, wherein the output data signal (Q3) has a plurality of rising and falling data edges (inherent to data signals) and the clock production circuit (Fig. 7) is operable to synchronize an arrival of the triggering clock edge at the downstream latch until after an arrival of the rising and falling data edges at the downstream latch (column 4, line 66 thru column 5, lines 25 and column 8, line 39 thru column 9, line 24 and column 9, lines 36 thru column 10, line 13).

Barkatullah fails to disclose the apparatus comprising: the microprocessor having a first supply voltage source; the input-output section having a second supply voltage source; a first level shifter, coupled to the selected section, to generate a level shifted data signal in response to the second data signal; a delay element and a second level shifter, coupled in series to the clock source, to generate a level shifted clock signal with a triggering clock edge in response to the clock signal.

Neal teaches a method and system (Fig. 6) for use in a computer system between a processor domain (140 within processor package) and a chipset for I/O of the processor (400) to be used for level-shifting between the two domains (processor voltage domain V2 and I/O domain V2) with a clock delaying mechanism (150) to synchronize clock triggering. Neal features a first domain/circuit (400) which produces data signals (401a-403a) that are transmitted through a level-shifter (101) to produces level-shifted data signals (401b-403b) (from domain V1 to domain V2; column 5, line 59 thru column 6, line 29). Neal further teaches a clock source (160) that is used by first domain (400) to synchronize data signals (401a-403a) wherein the clock signal is further level-shifted (via 101) and delayed via delay element (150) (column 5,



Art Unit: 2116

lines 15-58). Neal further teaches the additional benefit of providing a level-shifting technique to be used for a upgrading a board without need for redesigning the board (column 3, lines 1-4).

It would have been obvious to one of ordinary skill of the art having the teachings of Barkatullah and Neal at the time the invention was made, to modify the apparatus of Barkatullah to include the ability to level-shift both data and clock signals as well as delay the clock signal between domains for synchronization as taught by Neal. One of ordinary skill in the art would be motivated to make this combination of including the level-shifting of data and clock signals and deskewing of the clock signal in view of the teachings of Neal, as doing so would give the added benefit of providing a level-shifting technique to be used for a upgrading a board without need for redesigning the board (as taught by Neal above).

As to claim 11, Barkatullah in combination with Neal taught the apparatus in claim 10, as shown above. Neal further teaches the apparatus wherein the level shifted clock signal has a plurality of clock cycles with each of the clock cycles having a rising clock edge and a falling clock edge (inherent to clock signals).

Barkatullah further teaches the downstream latch has an open and a close state (inherent to flip-flops); and the downstream latch is switched from the close state to the open state by the triggering clock edge selected from the rising clock edge and the falling clock edge (column 9, line 36 thru column 10, line 43).

As to claims 14-15, they are directed to the apparatus of steps set forth in claim 11. Therefore, they are rejected for the same basis as set forth hereinabove.

As to claim 16, Barkatullah discloses a system, comprising: a microprocessor (100) including a central processing unit section (101) having a first clock domain (core clock); an

Art Unit: 2116

input-output section (105) having a second clock domain (bus clock); a clock source (102) to generate a clock signal (core clock and bus clock) (column 4, line 66 thru column 5, lines 25); and the CPU section being operable to generate a first data signal (core clock domain and D flip-flop outside of pad cell 831 in Fig. 8C hereinafter referred to as DFF1); a converter circuit including a flip-flop (D flip-flop on the left inside of pad cell 831 in Fig. 8C hereinafter referred to as DFF2), coupled to the clock source (core clock) and the selected section (DFF1), to generate a second data signal (Q output hereinafter referred to as Q2) in response to the clock signal and the first data signal (Q1); a clock production circuit (Fig. 7) coupled in series to the clock source (102), to generate a clock signal with a triggering clock edge (bus clock) in response to the clock signal (column 8, line 39 thru column 9, line 24); a downstream latch (D flip-flop on the right inside of pad cell 831 in Fig. 8C hereinafter referred to as DFF3) having an open and close state (inherent to flip-flops), a pair of inputs coupled to DFF2 and the clock production circuit (Fig. 7) and an output (Q output hereinafter referred to as Q3) coupled to the non-selected section of the CPU and I/O sections (external devices); the downstream latch adapted to generate an output data signal (Q3) in response to the data signal (Q2) and the triggering clock edge of the synchronized clock signal (bus clock) (column 9, lines 36 thru column 10, line 13); a source synchronous bus (external system bus), coupled to the I/O section (105), to receive the output data signal (Q3) and the synchronized clock signal (bus clock) (Barkatullah discloses the clock production circuits 102 producing core clocks and bus clocks that are synchronous and coupled to a system clock 110; column 4, line 66 thru column 5, line 25 and column 10, lines 14-24); an I/O module (105) coupled to the source synchronous bus (Fig. 1); and, wherein the output data signal (Q3) has a plurality of rising and falling data edges

Art Unit: 2116

(inherent to data signals) and the clock production circuit (Fig. 7) is operable to synchronize an arrival of the triggering clock edge at the downstream latch until after an arrival of the rising and falling data edges at the downstream latch (column 4, line 66 thru column 5, lines 25 and column 8, line 39 thru column 9, line 24 and column 9, lines 36 thru column 10, line 13).

Barkatullah fails to disclose the apparatus comprising: the microprocessor having a first supply voltage source; the input-output section having a second supply voltage source; a first level shifter, coupled to the selected section, to generate a level shifted data signal in response to the second data signal; a delay element and a second level shifter, coupled in series to the clock source, to generate a level shifted clock signal with a triggering clock edge in response to the clock signal.

Neal teaches a method and system (Fig. 6) for use in a computer system between a processor domain (140 within processor package) and a chipset for I/O of the processor (400) to be used for level-shifting between the two domains (processor voltage domain V2 and I/O domain V2) with a clock delaying mechanism (150) to synchronize clock triggering. Neal features a first domain/circuit (400) which produces data signals (401a-403a) that are transmitted through a level-shifter (101) to produces level-shifted data signals (401b-403b) (from domain V1 to domain V2; column 5, line 59 thru column 6, line 29). Neal further teaches a clock source (160) that is used by first domain (400) to synchronize data signals (401a-403a) wherein the clock signal is further level-shifted (via 101) and delayed via delay element (150) (column 5, lines 15-58). Neal further teaches the additional benefit of providing a level-shifting technique to be used for a upgrading a board without need for redesigning the board (column 3, lines 1-4).

Art Unit: 2116

It would have been obvious to one of ordinary skill of the art having the teachings of Barkatullah and Neal at the time the invention was made, to modify the apparatus of Barkatullah to include the ability to level-shift both data and clock signals as well as delay the clock signal between domains for synchronization as taught by Neal. One of ordinary skill in the art would be motivated to make this combination of including the level-shifting of data and clock signals and deskewing of the clock signal in view of the teachings of Neal, as doing so would give the added benefit of providing a level-shifting technique to be used for a upgrading a board without need for redesigning the board (as taught by Neal above).

As to claim 17, Barkatullah in combination with Neal taught the system in claim 16, as shown above. Neal further teaches the system wherein the I/O module is a selected one of a graphics and a video controller (column 3, lines 45-52).

As to claim 18, Barkatullah in combination with Neal taught the system in claim 16, as shown above. Neal further teaches the system wherein the level shifted clock signal has a plurality of clock cycles with each of the clock cycles having a rising clock edge and a falling clock edge (inherent to clock signals).

Barkatullah further teaches the downstream latch has an open and a close state (inherent to flip-flops); and the downstream latch is switched from the close state to open state by the triggering clock edge selected from the rising clock edge and the falling clock edge (column 9, line 36 thru column 10, line 43).

As to claims 21 and 22, they are directed to the system of steps set forth in claim 18. Therefore, they are rejected for the same basis as set forth hereinabove.

As to claim 28, Barkatullah discloses a converter circuit (Fig. 8C), comprising a flip-flop including a master latch (D flip-flop outside of pad cell 831 in Fig. 8C hereinafter referred to as DFF1) and an upstream slave latch (D flip-flop on the left inside of pad cell 831 in Fig. 8C hereinafter referred to as DFF2), to generate a latched data signal (Q output from DFF2 hereinafter referred to as Q2) in response to a clock signal (core clock) and an input data signal (from core clock domain shown in Fig. 8C; column 9, line 36 thru column 10, line 13); a clock production circuit (Fig. 7) to generate a synchronized clock signal (bus clock) having a triggering clock edge in response to the clock signal (column 8, line 39 thru column 9, line 24); and, a downstream slave latch (D flip-flop on the right inside of pad cell 831 in Fig. 8C hereinafter referred to as DFF3) having an open and a close state (inherent to flip-flops), coupled to DFF2 and the clock production circuit (Fig. 7), to generate an output data signal (Q output hereinafter referred to as Q3) in response to output data signal of DFF2 (Q2) and the triggering clock edge (bus clock); and, wherein the clock production circuit (Fig. 7) is adapted to synchronize an arrival of the triggering clock edge at the downstream slave latch until after an arrival of the signal transitions at the downstream slave latch (column 4, line 66 thru column 5, lines 25 and column 8, line 39 thru column 9, line 24 and column 9, lines 36 thru column 10, line 13).

Barkatullah fails to disclose: a first level shifter, coupled to the flip-flop, to generate a level shifted data signal in response to the latch data signal, with the level shifted data signal having a plurality of signal transitions; and delay element and a second level shifter coupled to the clock circuit.

Neal teaches a method and system (Fig. 6) for use in a computer system between a processor domain (140 within processor package) and a chipset for I/O of the processor (400) to

Art Unit: 2116

be used for level-shifting between the two domains (processor voltage domain V2 and I/O domain V2) with a clock delaying mechanism (150) to synchronize clock triggering. Neal features a first domain/circuit (400) which produces data signals (401a-403a) that are transmitted through a level-shifter (101) to produces level-shifted data signals (401b-403b) (from domain V1 to domain V2; column 5, line 59 thru column 6, line 29). Neal further teaches a clock source (160) that is used by first domain (400) to synchronize data signals (401a-403a) wherein the clock signal is further level-shifted (via 101) and delayed via delay element (150) (column 5, lines 15-58). Neal further teaches the additional benefit of providing a level-shifting technique to be used for a upgrading a board without need for redesigning the board (column 3, lines 1-4).

It would have been obvious to one of ordinary skill of the art having the teachings of Barkatullah and Neal at the time the invention was made, to modify the apparatus of Barkatullah to include the ability to level-shift both data and clock signals as well as delay the clock signal between domains for synchronization as taught by Neal. One of ordinary skill in the art would be motivated to make this combination of including the level-shifting of data and clock signals and deskewing of the clock signal in view of the teachings of Neal, as doing so would give the added benefit of providing a level-shifting technique to be used for a upgrading a board without need for redesigning the board (as taught by Neal above).

As to claim 30, Barkatullah in combination with Neal taught the converter circuit in claim 28, as shown above. Neal further teaches the converter circuit further comprising: a second level shifter (all inclusive within 101), coupled in series with the delay element, to voltage level shift the delayed clock signal (Fig. 6 and column 5, line 15 thru column 6, line 29).

As to claim 31, it is directed to the converter circuit of steps set forth in claim 30.

Therefore, it is rejected for the same basis as set forth hereinabove.

As to claim 32, Barkatullah in combination with Neal taught the converter circuit in claim 28, as shown above. Neal further teaches the converter circuit further comprising: a second level shifter (all inclusive within 101), coupled in series with the delay element, to voltage level shift the delayed clock signal (Fig. 6); and, wherein the delay element is adapted to introduce a predetermined delay having a duration exceeding a time period during which the rising and falling data edges are mismatched (column 5, line 15 thru column 6, line 29).

### ***Response to Arguments***

Applicant's arguments filed November 24, 2006 have been fully considered but they are not persuasive.

Applicant argues that neither Barkatullah nor Neal comprises a delay to avoid a period of signal mismatch caused by a level shifter. Examiner respectfully disagrees with this argument. Neal teaches a delay element (signal deskewer 150) that is coupled between a level shifter (101) and microprocessor (105). The level shifter in Neal is present to shift the voltage level of both data signals (401a, 402a, 403a) and clock signal (160). The deskewer (150) of Neal is present to add a delay (T-t) to compensate for delay (t) caused by the level shifter. Neal further teaches that this deskewing realigns falling and rising edges of the clock being delivered to the microprocessor (column 5, lines 16-58). Therefore, Barkatullah in combination with Neal does teach a delay element to avoid a period of signal mismatching such that the clock signal of

Art Unit: 2116

Barkatullah that is delivered to the flip-flop is delayed by the delay element of Neal to realign falling and rising edges of the clock delivered to said flip-flop.

The Applicant further argues that neither Barkatullah nor Neal comprises a downstream latch at the output of the of the level shifter operates with a clocking delay relative to the flip-flop at the input of the level shifter to block a period of mismatch in the level shifted data signal. Examiner asserts, as argued above, Barkatullah in combination with Neal does teach the downstream latch (DFF3 as presented in previous Office Action in Barkatullah) at the output of the level shifter of Neal and further operates to delay the clock mismatch of the clock signals (column 5, lines 16-58).

Also, Applicant argues that the downstream latch of Barkatullah (DFF3 noted above) is not the same as the latches described within the text cited (paragraph 16) from the Specification. However, the cited text in the Specification draws attention to a master-slave latch (42 comprising 44 and 46) that differs from downstream latch (56) that has a pair of inputs coupled to the first level shifter and the delay element. Barkatullah in combination with Neal does teach this limitation. Applicant further argues that a flip-flop is not a simple, single latch having an open and close state. However, the D flip-flops depicted in Barkatullah (column 9, line 9 thru column 10, line 13) are edge-triggered D flip-flops dependent on the clocks which inherently necessitates an open and close state (transparent and hold) ( see [http://en.wikipedia.org/wiki/Flip-flop\\_%28electronics%29](http://en.wikipedia.org/wiki/Flip-flop_%28electronics%29) herein included as reference).

Furthermore, Applicant argues that the second level shifter is not present to generate a level shifted clock signal. Examiner asserts that the level shifter (101) of Neal accommodates for all signals (401, 402 and 403) in addition to clock signal (160, 170) which internally necessitates



a second level shifter to accommodate the entire level shifter circuit (101) (column 5, line 40 thru column 6, line 3).

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., different clock frequencies in the domains) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). The Examiner would like to point out that Neal however, does not depict a clock generator that delivers different clock frequencies for the domains. Therefore, Barkatullah in combination with Neal does teach this limitation though it is not claimed.

Lastly, Barkatullah in combination with Neal also teaches that the domains do have different voltage levels and voltage level shifters in the Applicants' invention such that the level shifter of Neal provides this detail to the clock signal and data signals (as depicted in above arguments).

### ***Conclusion***

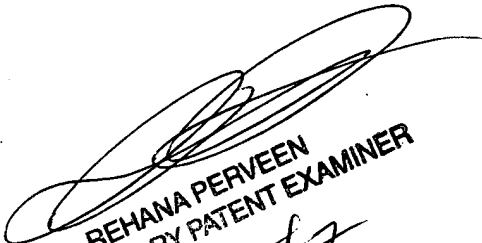
Any inquiry concerning this communication or earlier communications from the Examiner should be directed to James Sugent whose telephone number is (571) 272-5726. The Examiner can normally be reached on 8AM - 4PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Rehana Perveen can be reached on (571) 272-3676. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Art Unit: 2116

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at (866) 217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call (800) 786-9199 (IN USA OR CANADA) or (571) 272-1000.

James F. Sugent  
Patent Examiner, Art Unit 2116  
January 24, 2007

  
REHANA PERVEEN  
SUPERVISORY PATENT EXAMINER  
1/25/07